شبكة المعلومات الجامعية

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بسم الله الرحمن الرحيم

HANAA ALY

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جامعة عين شمس

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قسم

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HANAA ALY

AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Modelling and Simulation of Tunnel Field Effect Transistor (TFET)

A Thesis submitted in partial fulfilment of the requirements of the degree of

Master of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

by

Yasmin Yahia Ebrahim Morgan

Bachelor of Science in Electrical Engineering

(Electronics Engineering and Electrical Communications)

Faculty of Engineering, Modern Academy for Engineering and Technology, 2008

Supervised By

Prof. Dr. Mohamed Abdelhamid Abouelatta

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Cairo - (2021)

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Date:27 November 2021

Statement

This thesis is submitted as a partial fulfilment of Master of Science in Electrical Engineering Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Thesis Summary

Scaling down conventional MOSFETs has a vital challenge in electronic circuit design. The scaling of MOSFET depends not only on the device dimension and gate oxide thickness but also on the applied voltage. Unfortunately, down scaling has a negative effect on increasing the power consumption and other issues.

Several studies demonstrated to solve the MOSFETs problems but most of them are rendered impractical. Following the International Technology Roadmap for Semiconductors (ITRS), there is a vital need to reduce the device size. So, this led to Steep Slope devices like TFET devices to come into play as a problem-solving device.

TFET is promising device with low power consumption, low subthreshold swing, low applied voltage and low OFF current due to its band-to-band tunnelling mechanism. However, it has a low ON current and suffers from ambipolar effects. Several studies have been developed to increase the ON current and to reduce the ambipolar effect. These studies are based on either changing the structure of the device or changing the materials used in manufacturing, spacers, or gate dielectric.

In this work, Si-based DG (double gate) TFET devices are extensively studied by analytical calculations and simulations. Analytical calculations use MATLAB environment on the Si-DG TFET. It uses semi-analytical model considering depletion regions at both source/channel and drain/channel junctions. It also uses the SILVACO TCAD simulator in modelling. Here it is used to model a Tapered shape TFET, to study its impact on the ambipolar effect and ON current and ON/OFF current ratio.

Key words: DG-TFET, BTBT, *ON* Current, *SS*, ambipolar

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Table of Contents

List of Figures