Mona Maghraby

بسم اللّه الرحمن الرحيم

مركز الشبكات وتكنولوجيا المعلومات

قسم التوثيق الإلكتروني

Mona Maghraby

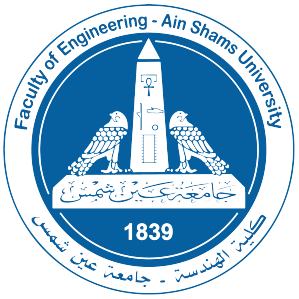
جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

نقسم باللّه العظيم أن المادة التي تم توثيقها وتسجيلها

علي هذه الأقراص المدمجة قد أعدت دون أية تغيرات



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Computer and Systems Engineering

Extending a Modern RISC Instruction Set for Performance Improvement

A Thesis submitted in partial fulfillment of the requirements of
Master of Science
(Computer and Systems Engineering)

by
Rizk Tawfik Rizk Tawfik
Bachelor of Science
(Computer and Systems Engineering)
Faculty of Engineering, Ain Shams University, 2016

Supervised By
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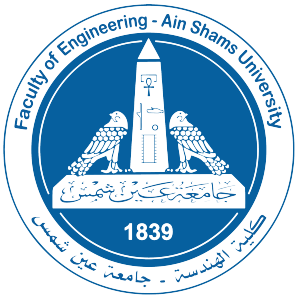
Cairo, 2022



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Statement

This thesis is submitted as a partial fulfillment of Master of Science in Computer and Systems Engineering, Faculty of Engineering, Ain shams University. The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

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Date: February 24, 2022

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Abstract

Multimedia applications, simulators and machine learning algorithms are examples of computer programs that require doing a set of repeated calculations over a large set of operands such as vectors and arrays. Improving the performance of such applications requires increasing the parallelism of those operations. Although replicating the CPU functional units would improve the performance, it would require increasing both the space and the complexity of the CPU. Adding to that, most of these applications usually requires less precision than the CPU precision, which results in computational power waste.

Almost all commercial processors nowadays have a vector extension which is responsible for executing a chain of instructions over a large set of operands efficiently. This extension is usually composed of multiple lanes, where each lane contains a variety of functional units. It also contains a large register file to exploit the locality of operands in executing these vector operations. However, not all these CPUs exploit the reduced precision we mentioned earlier.

In this thesis, RISC-V, a modern open-source RISC CPU, is extended to support integer operations fracturing within the Hwacha vector extension. The fracturing is done on two main components, the ALU and the integer multiplier unit. This modification allows up to two 32-bit operations and four 16-bit operations. The modification is implemented in Scala language on top of the Chisel Hardware framework. It is also designed with generality in mind, allowing any level of fracturing as long as the processor have the instruction support for that level of fracturing.

The thesis also goes through the implementation of different possible methods of fracturing integer multipliers, to suit different requirements of timing and fabrication space.

Summary

Increasing the performance of the CPU has been the focus of the digital industry since its inception. We expect new design, extension or feature every few years, but we expect speed improvement by the year. Some of these improvements relies on the fabrication technology, others rely on the improvement of the theory use, but in most cases, improvements come from increasing the level of parallelization.

In this thesis, we dive into improving the performance of integer mathematical and logic operations for operands with width less than processor datapath width. These improvements benefit applications that utilizes small precision operands such as multimedia and simulation applications.

The purpose of this improvement is to create generalized components that support any level of fracturing. This improvement would allow the full utilization of the components by preventing the need to extend the different operand sizes while allowing the calculation of more than one set of operands at a time. This would allow a 64-bit component such as an adder, a comparator or an integer multiplier to perform eight 8-bit operations rather than being limited to only one.

Vector processors are the best candidate to make use of fracturing since they support a variable length of vector operands. RISC-V processor with Hwacha vector extension was used for implementing the fracturing approaches. Usually the operand is stored in the widest supported width. This prevents the need of adding complex hardware to extend and shrink the operands on-the-fly. However, if the components support fracturing, multiple operands can be packed together in the register file and thus increasing the supported vector length.

We provide multiple implementations through this thesis for a fractured multiplier. They vary mainly in the number of multipliers. More multipliers infer more space and in contrast less multipliers would mean less space but higher complexity and more signal delay.

The thesis is divided into seven chapters as listed below:

Chapter 1 provides an introduction for the thesis. It contains the background and motivation for fracturing the processor execution unit.

Chapter 2 reviews the mathematical background required for designing the fractured modules, and the basic building blocks used in binary arithmetic.

Chapter 3 provides a brief introduction to the platform components that were used. It includes information about the RISC-V ISA, its implementation (RocketChip), its vector extension (Hwacha), the development language that was used for the implementation (Chisel), and the generator framework that integrates all of those (ShipYard).

Chapter 4 contains the approaches used for achieving the arithmetic components fracturing. The chapter is split into two main parts: ALU fracturing and integer multiplier fracturing. It covers the different approaches in-depth and highlighting the trade-off between the component delay versus the fabrication space.

Chapter 5 covers the methodology used in research from developing the component, unit testing, integration with core, integration testing and lastly the synthesis process.

Chapter 6 lists the evaluation results of the proposed implementations in terms of DSP count, their operation, ALUTs count and the frequency. The chapter concludes with a summarization table of the aforementioned implementations and provides the conclusion for this thesis.

Chapter 7 contains a summary of the findings, and the conclusion of this research based on the analysis results. It also describes the future work planned for this research.

Keywords: risc-v, hwacha, vector processor, fracturing, variable-width operations, fractured multiplier

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