

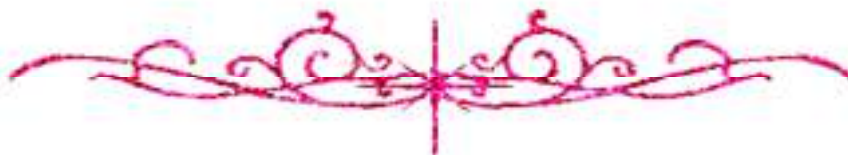
Safaa Mahmoud



بسم الله الرحمن الرحيم

مركز الشبكات وتكنولوجيا المعلومات

قسم التوثيق الإلكتروني



Safaa Mahmoud



جامعة عين شمس

التوثيق الإلكتروني والميكروفيلم

قسم

نقسم بالله العظيم أن المادة التي تم توثيقها وتسجيلها
على هذه الأقراص المدمجة قد أعدت دون أية تغييرات





AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

FPGA Implementation of Building Blocks of Conjugate Structure ACELP Speech Codec

A Thesis

Submitted in Partial Fulfillment for the Requirements of the
Degree of Master of Science in Electrical Engineering
(Electronics and Communication Engineering Department)

Submitted by

Heba Ahmed El-Sayed Ahmed

B.Sc degree in Electrical Engineering
HTI for Engineering and Technology, 2012

Supervised by

Prof. Dr. Abd El-Halim Abd El-Naby Zekry

Professor in Electronics and Electrical Communications Engineering Department,
Faculty of Engineering, Ain Shams University

Dr. Eman Mohammed Mahmoud

Lecturer in Electronics and Electrical Communications Engineering Department,
Modern Academy of Engineering and Technology

EGYPT, CAIRO

2019



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Name : Heba Ahmed El-Sayed Ahmed
**Thesis Title : FPGA Implementation of Building Blocks of Conjugate
Structure ACELP Speech Codec**
Degree : Master of Science in Electrical Engineering
Department: Electronics and Communications Engineering Department

Examiners' Committee

Name, Title and Affiliation

Signature

Prof. Dr. El-Sayed M. El-Rabaie

Professor in Electronics and Electrical Communications Engineering
Department, Faculty of Electronic Engineering, Menoufia University.

(Examiner)

.....

Prof. Dr. Wagdy Refaat Anis

Professor in Electronics and Electrical Communications Engineering
Department, Faculty of Engineering, Ain Shams University.

(Examiner)

.....

Prof. Dr. Abd El-Halim Abd El-Naby Zekry

Professor in Electronics and Electrical Communications Engineering
Department, Faculty of Engineering, Ain Shams University.

(Supervisor)

.....

Date : 2019 /12 / 30



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

STATEMENT

This thesis is submitted as a partial fulfillment of Master of Science. In Electrical Engineering, Faculty of Engineering, Ain shams University.

The author carried out the work included in this thesis, and no part of it has been submitted for a degree or a qualification at any other scientific entity.

Student name: Heba Ahmed El-Sayed Ahmed

Signature

Date/...../.....



AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Electronics Engineering and Electrical Communications

Researcher Data

Name : Heba Ahmed El-Sayed Ahmed
Date of birth : 22/6/1990
Place of birth : Suez, Egypt
Last academic degree : Bachelor of Science
Field of specialization : Electrical Engineering
(Electronics and Communication Engineering)
University issued the degree : HTI for Engineering and Technology
Date of issued degree : 2019
Current job : Teaching Assistant at Canal Higher Institute of
Engineering and Technology

Acknowledgment

All praise to *Allah* that good and blessings are done with his grace, who generous me in completing this work.

I would like to thank the examiners committee for their efforts in reviewing the thesis:

-Prof. Dr. El-Sayed Mahmoud El-Rabaie

-Prof. Dr. Wagdy Refaat Anis

No amount of thanks can express my gratitude and indebtedness to my supervisor Prof. Dr. Abdelhalim Zekry on his ongoing advice, support, encouragement and valuable suggestions. May Allah bless you. Allah gives you longevity, good health and good work.

I would like to express my sincere gratitude to my supervisor Dr. Eman Mohamed for her continuous help, guidance, advice, efforts and care. May Allah bless you.

My sincere gratitude and love to my parents, on everything in my life, continuous support, patience and their encouragement, May Allah blesses you both. Allah give both of you longevity, good health and good work.

Thesis Summary

Key words— CSACELP, Simulink, MATLAB, Visual Studio, DSK 6713, seg-SNR, LLR, MOS, PRAAT

As the emerging of real-time telecommunication systems over low bandwidth channels enforces constraints on the transmitted data rate while maintaining optimum speech quality at received destination, so speech coding techniques are being developed as waveform coder, parametric coder and hybrid coder. Hybrid coder is considered the optimal and satisfactory between speech coding algorithms to provide low bitrate with optimum speech quality.

This thesis presents one of hybrid speech coder types named Conjugate Structure Algebraic Code Excited Linear Prediction (CS-ACELP) which is nominated by International Tele-communication Union (ITU) as G.729. CS-ACELP encoder has two main stages per-frame analysis and per sub-frame analysis stages. The frame analysis stage of the Intended speech coder CS-ACELP is demonstrated by three main aspects.

Firstly, CS-ACELP is software simulated using SIMULINK model which was built from scratch based on MATLAB 2019. Four different acoustic speech signals are chosen as tested signals.

Secondly, CS-ACELP is hardware implemented on TMS320C6713 DSP kit based on C++ code generated from SIMULINK model. Additional optimizations are done to provide good reduction in the processing time by 8.564 us and reduction in the memory size used by 8% with acceptable speech quality.

Thirdly, a CS-ACELP encoder/decoder with International telecommunication union (ITU) MATLAB CSACELP code is developed, and then MATLAB coder (MEX tool) is used to generate C++ files that could compile and run it into desktop PCs. This desktop application is helpful in chat applications that require low bandwidth over the Internet and low connection speed.

The implemented CS-CELP tested signals are compared with the signals based on desktop application according to different measurements tests as objective measurements such as segmented signal-to-noise ratio (seg-SNR), log-likelihood ratio (LLR), and subjective measurements such as mean opinion score (MOS) and praat software test.

These testes are used to examine the speech quality of the synthesized signals based on the implemented C++ code generated from SIMULINK against reconstructed signals from desktop application.

This comparison proved that the reconstructed signal based on “analysis-by-synthesis” desktop application was better (less noise distortion) than the SIMULINK synthesis signal because of adding error parameters that done in the decoder side that help the decoder to estimate the original signal with minimum error as possible.

List of Contents

Chapter One (Introduction).....	1
1.1 Background.....	2
1.2 Thesis Motivation	2
1.3 Publications	3
1.4 Thesis Idea.....	3
1.5 Thesis Layout	4
1.6 Summary.....	5
Chapter Two (Speech Coding Terminology).....	6
2.1 Introduction	7
2.2 Human Speech Production	7
2.3 Speech Coding	8
2.4 Standardization	12
2.5 General CS-CELP Codec Encoder/Decoder Description	13
2.6 Summary.....	15
Chapter Three (CS-ACELP System Description).....	16
3.1 Introduction	17
3.2 Functional Description of the Encoder.....	17
3.3 Functional Description of the Decoder.....	39
3.4 Summary.....	47
Chapter Four (CS-ACELP SIMULINK Modeling)	48
4.1 Introduction	49
4.2 SIMULINK Building Blocks	49
4.3 SIMULINK Blocks Connection	59
4.4 SIMULINK Simulation	59
4.5 SIMULINK Code Generation	60
4.6 Summary.....	63
Chapter Five (Digital Signal Processing Implementation)	64
5.1 Introduction	65
5.2 TMS320C6713 Description and Functionality	65
5.3 DSP Tool	68
5.4 TI-TMS320C6713 Implementation Methodology	69
5.5 Summary.....	88
Chapter Six (Results and Discussion)	89
6.1 Introduction	90
6.2 Speech Performance Results	90

Chapter Seven (Conclusions and Future Work)..... 94

7.1 Conclusions 95

7.2 Future Work 95

REFERECES..... 96

Appendix A 101

Appendix B 107

List of Figures

Figure 2. 1 The speech human chain vocal.	7
Figure 2. 2 Block diagram of a speech coding system.	8
Figure 2. 3 Speech LPC filter mathematical model.	10
Figure 2. 4 LPC encoder diagram.	10
Figure 2. 5 LPC decoder diagram.	11
Figure 2. 6 Quality versus bitrate between three coder techniques	14
Figure 2. 7 CS-ACELP Encoder's Block Diagram.....	14
Figure 2. 8 CS-ACELP decoder's Block Diagram	15
Figure 3. 1 CS-CELP encoder.....	18
Figure 3. 2 LPC framing windowing.	19
Figure 3. 3 CS-ACELP decoder.....	40
Figure 3. 4 CS-ACELP decoder outline.....	41
Figure 4. 1 SIMULINK opening button.....	49
Figure 4. 2 SIMULINK Library browser.	50
Figure 4. 3 CS-ACELP frame-analysis SIMULINK model.	51
Figure 4. 4 LSF vector quantization building block.	52
Figure 4. 5 LSF vector conversion building block.....	52
Figure 4. 6 LSF weight computation building block.	53
Figure 4. 7 LSF / LAR conversion building block.....	53
Figure 4. 8 LSF interpolation building block.....	54
Figure 4. 9 LSF split vector quantization building block.....	54
Figure 4. 10 for iteration of LSF split vector quantization building block	55
Figure 4. 11 LSF interpolation building block.....	55
Figure 4. 12 weighting filter building block.	56
Figure 4. 13 gamma_1 of weighting filter computation building block.	56
Figure 4. 14 gamma_a of weighting filter computation building block.	57
Figure 4. 15 gamma b of weighting filter computation building block.	58
Figure 4. 16 pitch gain computation building block.	59
Figure 4. 17 SIMULINK simulation	60
Figure 4. 18 SIMULINK code generation	60
Figure 4. 19 SIMULINK solver code generation setup.	61
Figure 4. 20 SIMULINK hardware implementation setup.	61
Figure 4. 21 SIMULINK library code generation setting.	62
Figure 4. 22 SIMULINK code language setting.	62
Figure 4. 23 SIMULINK code generation.	63

Figure 5. 1 DSK TMS320C6713 kit board.	66
Figure 5. 2 DSK TMS320C6713 kit features Description.	67
Figure 5. 3 DSK TMS320C6713 kit functional Description.	68
Figure 5. 4 CCS Integrated Development Environment	69
Figure 5. 5 CCS creating a project.	70
Figure 5. 6 CCS adding .C and .h files to the project	70
Figure 5. 7 CCS building a project (a)	71
Figure 5. 8 CCS building a project (b)	71
Figure 5. 9 Load the project	72
Figure 5. 10 CCS program level steps	73
Figure 5. 11 C6000 Compiler setting.....	73
Figure 5. 12 CCS target configuration setting	75
Figure 5. 13 CCS naming the target configuration file	75
Figure 5. 14 CCS target configuration file setting	76
Figure 5. 15 CCS debugging procedure step1	76
Figure 5. 16 CCS debugging procedure step 2	77
Figure 5. 17 CCS debugging procedure step 3	77
Figure 5. 18 CCS profiling procedure step 1	78
Figure 5. 19 CCS profiling procedure step 2	78
Figure 5. 20 CCS profiling view code procedure step 1	79
Figure 5. 21 CCS profiling view code procedure step 2	79
Figure 5. 22 CCS code tracing procedure step 1	80
Figure 5. 23 CCS code tracing procedure step 2.....	81
Figure 5. 24 Flowchart of the python code compares the mat file with DSK file producing the error	83
Figure 5. 25 Comparison between the optimized pre-emphasis signal "Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation.	84
Figure 5. 26 Comparison between the optimized auto-correlation signal "Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation.	84
Figure 5. 27 Comparison between the optimized Levinson signal "Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation.	85
Figure 5. 28 Comparison between the optimized LAR signal "Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation.	85
Figure 5. 29 Comparison between the optimized qlsf signal "Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation.	86
Figure 5. 30 Comparison between the optimized LSF interpolated signal "Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation.	86
Figure 5. 31 Comparison between the optimized RC interpolated signal "Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation.	87
Figure 5. 32 Comparison between the optimized (LSF/LSP to LPC) interpolated signal "Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation.	87
Figure 5. 33 Comparison between the optimized (Synthesis block) interpolated signal "Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation.	88

Figure 5. 34 Comparison between the optimized (Weighting filter) interpolated signal
"Male_syn.wav" obtained from SIMULINK versus obtained from DSK implementation. 88

Figure 6. 1 Synthesis signals bar diagram for the MOS Score. 92

Figure 6. 2 "Male.wav" original file formant plot. 93

Figure 6. 3 "Male_syn.wav" synthesis file formants plot. 93

Figure 6. 4 "Male_rec.wav" reconstructed file formants plot. 93

List of Tables

Table 2. 1	Differents speech coder algorithms.....	12
Table 3. 1	Compiler options results	33
Table 5. 1	CS-ACELP Total memory used inside the internal RAM, comparison between ordinary and optimized code.	74
Table 5. 2	CS-ACELP Average cycles inclusive and exclusive comparison for the ordinary code against the optimized code.	80
Table 6. 1	The segSNR evaluation test of different implemented and simulated CS-CELP..	91
Table 6. 2	The LLR evaluation test of different simulated and implemented CS-CELP	92

List of Abbreviations

CELP	Code-Excited Linear Prediction
CODEC	Compression/Decompression
CS-ACELP	Conjugate-Structure Algebraic CELP
DSP	Digital Signal Processing
LAR	Log Area Ratio
LLR	Log Likelihood Ratio
LP	Linear Predictive
LSF	Line Spectral Frequency
LSP	Line Spectral Pair
MA	Moving Average
MOS	Mean Opinion Score
MSB	Most Significant Bit
MSE	Mean-Squared Error
MSVQ	Multistage VQ
Seg-SNR	Segmented signal-to-noise ratio
SNR	Signal to Noise Ratio
SVQ	Split VQ
VQ	Vector Quantization
WCDMA	Wide Band Code Division Multiple Access.